Penguin Edge™ MVME7100ET

Programmer’s Reference

P/N: 6806800K88D

August 2022

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About this Manual

Overview of Contents

This manual is divided into the following chapters and appendices:

Chapter 1, Introduction on page 7, provides a brief product description and a block diagram showing the architecture of the MVME7100ET Single Board Computer.

Chapter 2, Memory Maps on page 13, provides information on the memory maps of the board.

Chapter 3, Register Descriptions on page 17, contains status registers for the system resources.

Chapter 4, Programming Details on page 43, includes additional programming information for the MVME7100ET.

Appendix A, Programmable Configuration Data on page 59, provides additional programming information including IDSEL mapping, interrupt assignments for the MC864*x*D interrupt controller, Flash memory, two-wire serial interface addressing, and other device and system considerations.

Appendix B, Related Documentation on page 79, provides a listing of related Penguin Solutions manuals, vendor documentation, and industry specifications.

Abbreviations

This document uses the following abbreviations:

Acronym	Description
ASCII	American Standard Code for Information Interchange
CRC	Cyclic Redundancy Check
EEPROM	Electrically Erasable Programmable Read Only Memory
FRU	Field Replaceable Unit
Flash	Flash Memory
GB	Gigabyte
HEX	Hexadecimal
Hz	Hertz
IPMI	Intelligent Platform Management Interface
MB	Megabyte

Acronym	Description
Mfg	Manufacturing
SPD	Serial Presence Detect
VPD	Vital Product Data

Conventions

The following table describes the conventions used throughout this manual:

Notation	Description
`0x00000000`	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
`0b0000`	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands. `Sample of Programming used in a table (9pt)`
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury

Notation	Description
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	Indicates a hot surface that could result in moderate or serious injury
	Indicates an electrical situation that could result in moderate injury or death
	Indicates that when working in an ESD environment care should be taken to use proper ESD practices
	No danger encountered, pay attention to important information

Summary of Changes

This manual has been revised and replaces all prior editions.

Part Number	Publication Date	Description
6806800K88D	August 2022	Rebrand to Penguin Solutions.
6806800K88C	October 2019	Rebrand to SMART Embedded Computing template
6806800K88B	June 2014	Rebranded to Artesyn template.
6806800K88A	September 2010	First Release

Introduction

1.1 Overview

This chapter briefly describes the board level hardware features of the MVME7100ET single board computer. Refer to the MC864xD Reference Manual listed in *Appendix B, Related Documentation on page 79*, for more details and programming information.

1.2 Ordering and Support Information

Refer to the MVME7100 data sheet for a complete list of available variants and accessories. Refer to *Appendix B, Related Documentation on page 79* or consult your local Penguin Solutions™ sales representative for the availability of other variants.

For technical assistance, documentation, or to report product damage or shortages, contact your local Penguin Solutions sales representative or visit our web site at *https://www.penguinsolutions.com/edge/support/*.

NOTE: The IPMC712 and IPMC761 I/O modules are not supported on the MVME7100ET SBC.

1.3 Features

The following table provides a summary of the features common to all board variations.

Table 1-1 Features List

Function	Features
Processor / Host Controller / Memory Controller	One MC864xD Integrated Processor Two e600 cores with integrated L2 Core frequency of 1.067 or 1.33 GHz One integrated four channel DMA controller Two integrated PCIE interfaces Four integrated 10/100/1000 Ethernet controllers One integrated DUART Two integrated I2C controllers One integrated Programmable Interrupt Controller One integrated Local Bus Controller Two integrated DDR2 SDRAM controllers
System Memory	Two banks of DDR2 SDRAM with ECC 2 GB or 4 GB
I^2C	One 8 KB VPD serial EEPROM Two 64 KB user configuration serial EEPROMs One Real Time Clock (RTC) with removable battery Dual temperature senso Two SPDs for memory Connection to XMCspan and RTM
NOR Flash	128 MB soldered flash with two alternate 1 MB boot sectors selectable via hardware switch H/W switch or S/W bit write protection for entire logical bank
NAND Flash	Up to two devices available: 4 GB - 1 device 8 GB - 2 device

Table 1-1 Features List (continued)

Function	Features
NVRAM	One 512 KB MRAM extended temperature range Two 64 KB serial EEPROMs
PCI-E	8X Port to XMC Expansion 8X Port to 5 Port PCI Express switch
I/O	One front panel mini DB-9 connector for front I/O: one serial channel Two front panel RJ-45 connectors with integrated LEDs for front I/O: two 10/100/1000 Ethernet channels PMC site 1 front I/O and rear P2 I/O PMC site 2 front I/O
Ethernet	Four 10/100/1000 MC864xD Ethernet channels: Two front panel Ethernet connectors Two channels for rear P2 I/O
Serial Interface	One 16550-compatible, 9.6 to 115.2 Kbaud, MC864xD, asynchronous serial channel: one channel for front panel I/O One quad UART (QUART) controller to provide four 16550-compatible, 9.6 to 115.2 Kbaud, asynchronous serial channels: four channels for rear P2 I/O
Timers	Four 32-bit MC864xD timers Four 32-bit timers in a PLD
Watchdog Timer	One watchdog timer in PLD
VME Interface	VME64 (ANSI/VITA 1-1994) compliant (3 row backplane 96-pin VME connector) VME64 Extensions (ANSI/VITA 1.1-1997) compliant (5 row backplane 160-pin VME connector) 2eSST (ANSI/VITA 1.5-2003) compliant Two five-row P1 and P2 backplane connectors One Tsi148 VMEbus controller
Form Factor	Standard 6U VME, one slot

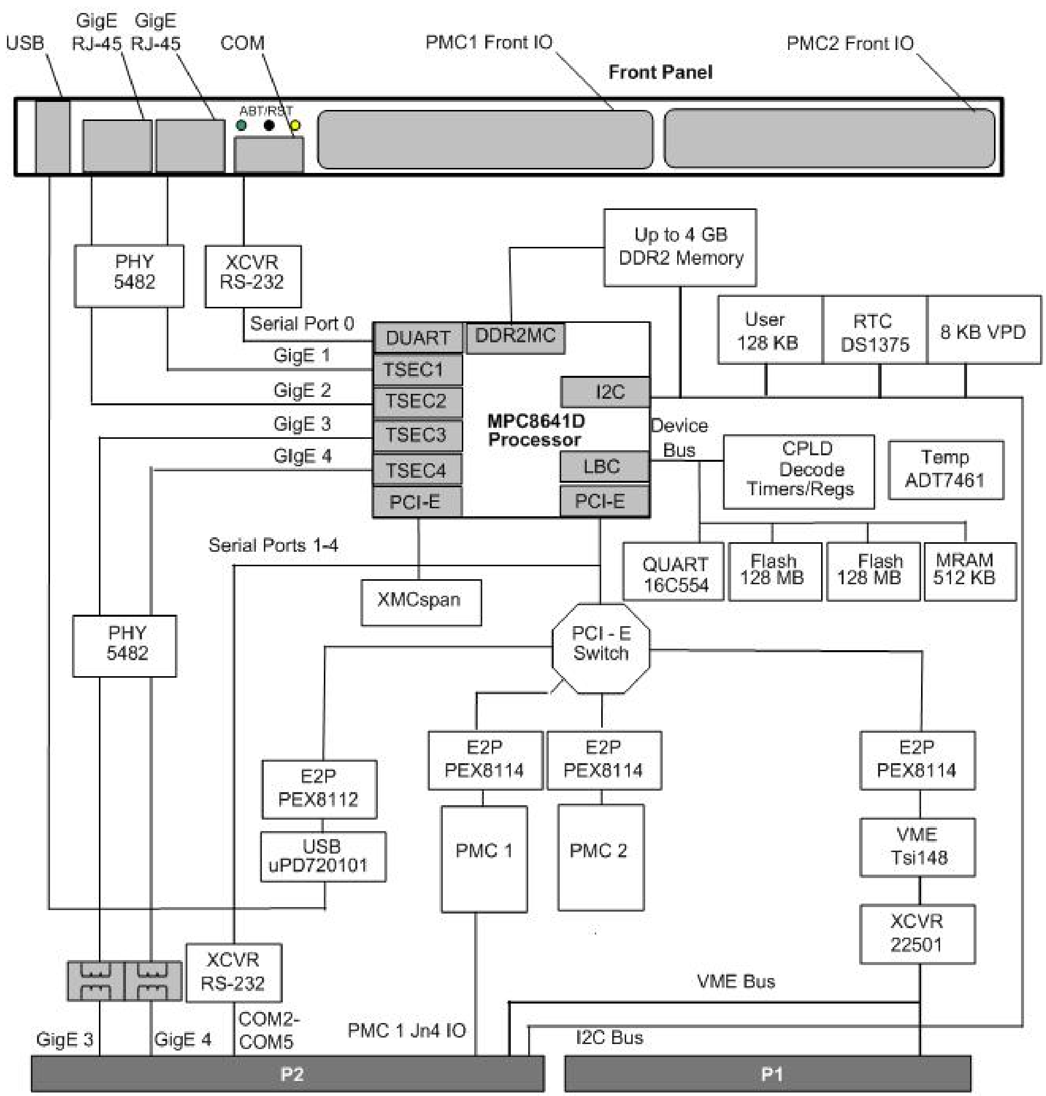
Table 1-1 Features List (continued)

Function	Features
Miscellaneous	One front panel RESET/ABORT switch Six front panel status indicators: Two 10/100/1000 Ethernet link/speed and activity (4 total) Board fail User S/W controlled LED Planar status indicators One standard 16-pin JTAG/COP header Boundary scan support Switches for VME geographical addressing in a three-row backplane
Software Support	VxWorks OS support Linux OS support

1.4 Block Diagram

The following figure is a block diagram of the MVME7100ET architecture.

Figure 1-1 Block Diagram



1.5 Functional Description

The MVME7100ET is a VMEbus board based on the MC8640D and MC8641D Integrated Processors. The MVME7100ET provides 2eSST VMEbus interfaces, dual 64-bit/100MHz PMC sites, 128MB of NOR flash and up to 8GB of NAND flash, up to 4GB of DDR2 SDRAM, quad 10/100/1000 Ethernet, and five serial ports. The MVME7100ET supports front and rear I/O with access to the rear I/O via the MVME7100ET transition module.

The MVME7100ET provides front panel access to one serial port with a mini DB-9 connector and two 10/100/1000 Ethernet ports with two RJ-45 connectors. The front panel includes a fail indicator LED, user-defined indicator LED, and a reset/abort switch.

The MVME721ET transition module provides rear panel access to four serial ports with one RJ-45 connector per port and two 10/100/1000 Ethernet ports with two RJ-45 connectors. The RTM also provides two planar connectors for one PIM with front I/O.

The block diagram for the MVME7100ET SBC is shown in *Figure 1-1*.

1.6 Programming Model

The MVME7100ET programming model is based on the MC864xD local memory map, which refers to the 36-bit address space seen by the processor as it accesses memory and I/O space. DMA engines also see the same local memory map. All memory accessed by the MC864xD DDR2 SDRAM and local bus memory controllers exists in this memory map in addition to all memory mapped configuration, control, and status registers. Memory maps and registers are described in *Chapter 2, Memory Maps* and *Chapter 3, Register Descriptions*.

Memory Maps

2.1 Overview

The following sections describe the memory maps for the MVME7100ET. Refer to the *MC864xD Reference Manual* for additional details and/or programming information.

2.1.1 Default Processor Memory Map

The following table describes a default memory map from the point of view of the processor after a processor reset.

Table 2-1 Default Processor Address Map

Processor Address		Size	Definition	Notes
Start	End			
0000 0000	FF6F FFFF	4087 M	Not mapped	
FF70 0000	FF7F FFFF	1 M	MC864xD CCSR Registers	
FF80 0000	FFFF FFFF	8 M	Flash	1

1. The e600 core fetches the first instruction from FFF0 0100 following a reset.

2.1.2 Suggested Processor Memory Map

The following table describes a suggested physical memory map from the point of view of the processor. This table reflects the address map implemented by the board level firmware at release time.

Table 2-2 Suggested Processor Address Map

Processor Address		Size	Definition	Notes
Start	End			
0000 0000	top_dram - 1	dram_size (2 GB max.	System Memory (on-board DRAM)	
8000 0000	CFFF FFFF	1.25 GB	PCI 0 Memory Space / VME	
D000 0000	DFFF FFFF	256 MB	PCI 1 Memory Space	
E000 0000	EFFF FFFF	256 MB	Not used	

Table 2-2 Suggested Processor Address Map (continued)

Processor Address		Size	Definition	Notes
Start	End			
F000 0000	F07F FFFF	8 MB	PCI 0 I/O Space	
F080 0000	F0FF FFFF	8 MB	PCI 1 I/O Space	
F100 0000	F10F FFFF	1 MB	MC864xD CCSR	
F110 0000	F1FF FFFF	15 MB	Not used	
F200 0000	F200 FFFF	64 KB	Status/Control Registers	
F201 0000	F201 FFFF	64 KB	UARTs	
F202 0000	F202 FFFF	64 KB	Timers	
F203 0000	F203 FFFF	64 KB	NAND Flash	
F204 0000	F23F FFFF	3.9 MB	Not used	
F240 0000	F247 FFFF	512 KB	MRAM	
F248 0000	F7FF FFFF	91.5 MB	Not used	
F800 0000	FFFF FFFF	128 MB	NOR Flash	
I_00000000	I_7FFFFFFF	2 GB	Second bank of RAM	1

1. Only on versions with 64B of RAM.

2.1.3 PCI Memory Map

The following table is the suggested PCI memory map for each PCI bus. This table reflects the address map implemented by the board level firmware at release time.

Table 2-3 PCI Memory Map

PCI Address		Size	Definition	Notes
Start	End			
0x00000000	top_dram - 1	dram_size	System Memory (on-board DRAM)	1
0x80000000	0xCFFFFFFF	0x50000000	PCI 0 Memory Space	1

Table 2-3 PCI Memory Map (continued)

PCI Address		Size	Definition	Notes
Start	End			
0x00000000	0x007FFFFF	0x00800000	PCI 0 I/O Space	1
0xD0000000	0xDFFFFFFF	0x10000000	PCI 1 Memory Space	1
0x00000000	0x007FFFFF	0x00800000	PCI 1 I/O Space	1

1. CHRP-based addressing

2.1.4 VME Memory Map

The MVME7100ET is fully capable of supporting both the PReP and the CHRP VME Memory Map examples with RAM size limited to 2GB.

Register Descriptions

3.1 Overview

System resources including system control and status registers, external timers, and the QUART are mapped into a 16 MB address range accessible from the MVME7100ET local bus via the MC864xD LBC. The memory map is defined in the following table including the LBC bank chip select used to decode the register.

Table 3-1 System I/O Memory Map

Address	Definition	LBC Bank/Chip Select	Notes
F200 0000	System Status Register	4	3
F200 0001	System Control Register	4	3
F200 0002	Status Indicator Register	4	3
F200 0003	NOR Flash Control/Status Register	4	3
F200 0004	Interrupt Register 1	4	3
F200 0005	Interrupt Register 2	4	3
F200 0006	Presence Detect Register	4	3
F200 0010	NAND Flash Chip 1 Control Register	4	3
F200 0011	NAND Flash Chip 1 Select Register	4	3
F200 0012	Reserved	4	1
F200 0013	Reserved	4	1
F200 0014	NAND Flash Chip 1 Presence Register	4	3
F200 0015	NAND Flash Chip 1 Status Register	4	3
F200 0016	Reserved	4	1
F200 0017	Reserved	4	1
F200 0018	NAND Flash Chip 2 Control Register	4	3
F200 0019	NAND Flash Chip 2 Select Register	4	3
F200 001A	Reserved	4	1

Table 3-1 System I/O Memory Map (continued)

Address	Definition	LBC Bank/Chip Select	Notes
F200 001B	Reserved	4	1
F200 001C	NAND Flash Chip 2 Presence Register	4	3
F200 001D	NAND Flash Chip 2 Status Register	4	3
F200 001E	Reserved	4	1
F200 001F	Reserved	4	1
F200 0020	Watch Dog Timer Load	4	3
F200 0021	Reserved	4	1
F200 0022	Reserved	4	1
F200 0023	Reserved	4	1
F200 0024	Watchdog Timer Control (32 bits)	4	3
F200 0028	Reserved (32 bits)	4	1
F200 002C	Reserved (32 bits)	4	1
F200 0030	PLD Revision	4	3
F200 0031	Reserved	4	1
F200 0032	Reserved	4	1
F200 0033	Reserved	4	1
F200 0034	PLD Date Code (32 bits)	4	3
F200 0038	Test Register 1 (32 bits)	4	3
F200 003C	Test Register 2 (32 bits)	4	3
F200 0018 - F200 0FFF	Reserved		1
F201 1000 - F201 1FFF	COM 2 (QUART channel 1)	5	

Table 3-1 System I/O Memory Map (continued)

Address	Definition	LBC Bank/Chip Select	Notes
F201 2000 - F201 2FFF	COM 3 (QUART channel 2)	5	
F201 3000 - F201 3FFF	COM 4 (QUART channel 3)	5	
F201 4000 - F201 4FFF	COM 5 (QUART channel 4)	5	
F201 5000 - F201 FFFF	Reserved		1
F202 0000	External PLD Tick Timer Prescaler Register	6	2
F202 0010	External PLD Tick Timer 1 Control Register	6	2
F202 0014	External PLD Tick Timer 1 Compare Register	6	2
F202 0018	External PLD Tick Timer 1 Counter Register	6	2
F202 001C	Reserved	6	2
F202 0020	External PLD Tick Timer 2 Control Register	6	2
F202 0024	External PLD Tick Timer 2 Compare Register	6	2
F202 0028	External PLD Tick Timer 2 Counter Register	6	2
F202 002C	Reserved	6	2
F202 0030	External PLD Tick Timer 3 Control Register	6	2
F202 0034	External PLD Tick Timer 3 Compare Register	6	2
F202 0038	External PLD Tick Timer 3 Counter Register	6	2
F202 003C	Reserved	6	2
F202 0040	External PLD Tick Timer 4 Control Register	6	2
F202 0044	External PLD Tick Timer 4 Compare Register	6	2
F202 0048	External PLD Tick Timer 4 Counter Register	6	2

Table 3-1 System I/O Memory Map (continued)

Address	Definition	LBC Bank/Chip Select	Notes
F202 004C - F2FF FFFF	Reserved	6	1
F203 0000	NAND Chip 1 Data Register	2	3
F203 0001 - F203 0FFF	Reserved	2	1
F203 1000	NAND Chip 2 Data Register	2	3
F203 1001 - F203 FFFF	Reserved	2	1

NOTES:

1. Reserved for future implementation.
2. 32-bit write only.
3. Byte read/write capable.

3.1.1 System Status Register

The MVME7100ET has a System Status Register that is a read only register used to provide general board status information.

Table 3-2 System Status Register

REG	System Status Register - 0xF200 0000							
BIT	7	6	5	4	3	2	1	0
Field	SW8	MASTER WP	PMC 133	Core 1 OFFSET	SAFE_S TART	PEX 8525 ERROR	BD_TYPE	
OPER	R							
RESET	X	X	X	X	X	0	0	0

BD_TYPE — Board Type. These bits indicate the board type.

00: VME SBC

	01: PrPMC
	10-11: reserved
PEX8525ERROR	PEX8525 Fatal Error. This bit reflects the Fatal Error signal from the PEX8525. A set condition indicates the error signal is active.
SAFE_START	ENV Safe Start. This bit reflects the current state of the ENV safe start select switch. A cleared condition indicates that the ENV settings programmed in NVRAM should be used by the firmware. A set condition indicates that firmware should use the safe ENV settings.
Core 1 OFFSET	Core 1 Low Memory Offset. This bit reflects the current state of Core 1 Low Memory Offset switch. A cleared condition indicates the switch is off. A set condition indicates the switch is on. When this switch is on, real address A in the range of 0 to 256 MBytes-1 is translated to address A +256 MBytes. When this switch is off, the address is not translated.
PMC133	PMC133. This bit reflects the current state of the PMC 133 MHz switch. A Cleared condition indicates the switch is off. A set condition indicates the switch is on. When this switch is on, the maximum PMC clock frequency is 133 MHz. When this switch is off, the maximum PMC clock frequency is 100 MHz.
MASTER WP	MASTER WP. This bit reflects the current state of the MASTER WP switch. A cleared condition indicates the switch is off. A set condition indicates the switch is on. When this switch is on, the NOR FLASH, NAND FLASH, MRAM and I^2C EPROMs are write protected. When this switch is off, NOR FLASH, NAND FLASH, MRAM and I^2C EPROMs are not write protected by this function. Other switches and control bits may write protect individual devices.
SW8	SW8. This bit reflects the current state of SW8. A cleared condition indicates the switch is off. A set condition indicates the switch is on.

3.1.2 System Control Register

The MVME7100ET has a System Control Register that provides general board control bits.

Table 3-3 System Control Register

REG	**System Control Register - 0xF200 0001**							
BIT	7	6	5	4	3	2	1	0
Field	BRD_RST			RSVD	RSVD	RSVD	EEPROM_WP	RSVD
OPER	R/W			R	R	R	R/W	R
RESET	0	0	0	0	0	0	1	0

EEPROM_WP	EEPROM Write Protect. This bit is to provide protection against inadvertent writes to the on-board EEPROM devices. Clearing this bit will enable writes to the EEPROM devices. Setting this bit write protects the devices. The devices are write protected following a reset.
BRD_RST	Board Reset. These bits are used to force a hard reset of the board. If a pattern is written in bits 5-7 where bit 7 is set, bit 6 is cleared, and bit 5 is set (101), a hard reset is generated. Any other pattern written in bits 5-7, does not generate a hard reset. These bits are cleared automatically when the board reset has been completed. These bits are always cleared during a read.
RSVD	Reserved for future implementation.

3.1.3 Status Indicator Register

The MVME7100ET provides a Status Indicator Register that may be read by the system software to determine the state of the on-board status indicator LEDs or written to by system software to illuminate the corresponding on-board LEDs.

Table 3-4 Status Indicator Register

REG	Status Indicator Register - 0xF200 0002							
BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	USR3	USR2	USR1 Y	USR1 R
OPER	R	R	R	R	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	1

USR1R User LED 1 RED. This bit is used to control the USR1 bi-color LED located on the front panel. A set condition illuminates the red segment of the front panel LED and a cleared condition extinguishes the red segment of the front panel LED.

USR1Y User LED 1 Yellow. This bit is used to control the USR1 bi-color LED located on the front panel. A set condition illuminates the yellow segment of the front panel LED and a cleared condition extinguishes the yellow segment of the front panel LED.

USR2_LED User LED 2. This bit is used to control the planar USR2 LED. A set condition illuminates the LED and a cleared condition extinguishes the LED.

USR3_LED User LED 3. This bit is used to control the planar USR3 LED. A set condition illuminates the LED and a cleared condition extinguishes the LED.

RSVD Reserved for future implementation

3.1.4 NOR Flash Control/Status Register

The MVME7100ET Flash Control/Status Register provides software controlled bank write protect and map select functions as well as boot block select, bank write protect, and activity status for the NOR flash.

Table 3-5 NOR Flash Control/Status Register

REG	NOR Flash Control/Status Register - 0xF200 0003							
BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	MAP_SEL	F_WP_SW	F_WP_HW	FBT_BLK_SEL	FLASH_RDY
OPER	R	R	R	R/W	R/W	R	R	R
RESET	0	0	0	0	1	X	X	1

FLASH_RDY Flash Ready. This bit provides the current state of the NOR flash devices Ready/Busy# pins. These open drain output pins from each flash device are wire OR'd to form Flash Ready. Refer to the appropriate flash device data sheet for a description on the function of the Ready/Busy# pin.

FBT_BLK_SEL Flash Boot Block Select. This bit reflects the current state of the Boot Block B Select switch. A cleared condition indicates that boot block A is selected and mapped to the highest address (see Figure 4). A set condition indicates that boot block B is selected and mapped to the highest address (see *Figure 3-1*).

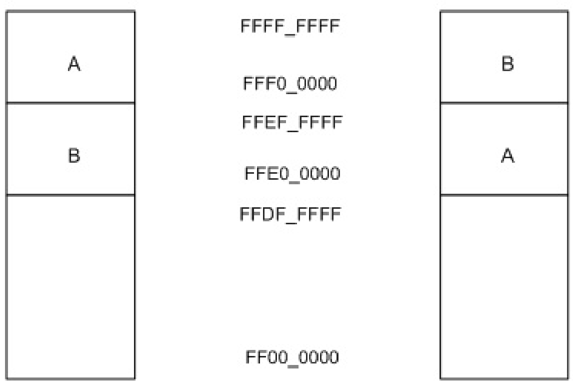
F_WP_HW Hardware Flash Bank Write Protect switch status. This bit reflects the current state of the FLASH BANK WP switch. A set condition indicates that the NOR Flash bank is write protected. A cleared condition indicates that the flash bank is not write protected.

F_WP_SW Software Flash Bank Write Protect. This bit provides software-controlled protection against inadvertent writes to the flash memory devices. A set condition indicates that the entire flash is write-protected. A cleared condition indicates that the flash bank is not write-protected, only when the HW write-protect bit is not set. This bit is set during reset and must be cleared by the system software to enable writing of the flash devices.

MAP_SEL Memory Map Select. When this bit is cleared, the flash memory map is controlled by the Flash Boot Block Select switch (see the MVME7100ET Installation and Use manual for switch settings). When the Map Select bit is set, boot block A is selected and mapped to the highest address (see *Figure 3-1*).

RSVD Reserved for future implementation.

Figure 3-1 Boot Flash Bank



3.1.5 Interrupt Register 1

The MVME7100ET provides an Interrupt Register that may be read by the system software to determine which of the Ethernet PHYs originated their combined (OR'd) interrupt.

Table 3-6 Interrupt Register 1

REG	**Interrupt Register 1 - 0xF200 0004**							
BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	PHY4	PHY3	PHY2	PHY1
OPER	R							
RESET	0	0	0	0	0	0	0	0

PHY1	TSEC1 PHY Interrupt. If cleared, the TSEC1 interrupt is not asserted. If set, the TSEC1 interrupt is asserted.
PHY2	TSEC2 PHY Interrupt. If cleared, the TSEC2 interrupt is not asserted. If set, the TSEC2 interrupt is asserted.
PHY3	TSEC3 Interrupt. If cleared, the TSEC3 interrupt is not asserted. If set, the TSEC4 interrupt is asserted.
PHY4	TSEC4 Interrupt. If cleared, the TSEC4 interrupt is not asserted. If set, the FEC interrupt is asserted.
RSVD	Reserved for future implementation.

3.1.6 Interrupt Register 2

The RTC, TEMP sensor and Abort switch interrupts are OR'd together. The MVME7100ET provides an Interrupt Register that may be read by the system software to determine which device originated the interrupt. This register also includes bits that allow the interrupt sources to be masked.

Table 3-7 Interrupt Register 2

REG	Interrupt Register 2 - 0xF200 0005							
BIT	7	6	5	4	3	2	1	0
Field	RSVD	RTC Mask	TEMP Mask	ABORT Mask	RSVD	RTC Status	TEMP Status	ABORT Status
OPER	R	R/W			R			
RESET	0	1	1	1	0	X	X	0

ABORT Status	ABORT Status. This bit reflects the current state of the on-board abort signal. This is a debounced version of the abort switch and may be used to determine the state of the abort switch. A cleared condition indicates that the abort switch is not depressed while a set condition indicates that the abort switch is asserted.
TEMP Status	TEMP Status. If cleared, the Temperature sensor output is not asserted. If set, the Temperature sensor output is asserted.
RTC Status	RTC Status. If cleared, the RTC output is not asserted. If set, the RTC output is asserted.

ABORT Mask	ABORT Mask. This bit is used to mask the abort switch output. If this bit is cleared, the abort switch output is enabled to generate an interrupt. If the bit is set, the abort switch output is disabled from generating an interrupt.
TEMP Mask	TEMP Mask. This bit is used to mask the ADT7461 temperature sensor thermostat output. If this bit is cleared, the thermostat output is enabled to generate an interrupt. If the bit is set, the thermostat output is disabled from generating an interrupt.
RTC Mask	RTC Mask. This bit is used to mask the RTC output. If this bit is cleared, the RTC output is enabled to generate an interrupt. If the bit is set, the RTC output is disabled from generating an interrupt.
RSVD	Reserved for future implementation.

3.1.7 Presence Detect Register

The MVME7100ET provides a Presence Detect Register that may be read by the system software to determine the presence of optional devices.

Table 3-8 Presence Detect Register

REG	**Presence Detect Register - 0xF200 0006**							
BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	ERDY2	ERDY1	RSVD	PEP	PMC2P	PMC1P
OPER	R							
RESET	0	0	0	0	0	X	X	X

PMC1P	PMC Module 1 Present. If cleared, there is no PMC module installed in site 1. If set, the PMC module is installed.
PMC2P	PMC Module 2 Present. If cleared, there is no PMC module installed in site 2. If set, the PMC module is installed.
XEP	XMCspan Present. If cleared, there is no XMCspan module installed. If set, the XMCspan module is installed.
ERDY1	EREADY1. Indicates that the PrPMC module installed in PMC site 1 is ready for enumeration when set. If cleared, the PrPMC module is not ready for enumeration. If no PrPMC is installed, this bit is always set.

ERDY2	EREADY2. Indicates that the PrPMC module installed in PMC site 2 is ready for enumeration when set. If cleared, the PrPMC module is not ready for enumeration. If no PrPMC is installed, the bit is always set.
RSVD	Reserved for future implementation.

3.1.8 NAND Flash Chip 1 Control Register

The MVME7100ET provides a Control Register for the NAND Flash device.

Table 3-9 NAND Flash Chip 1 Control Register

REG	NAND Flash Chip 1 Control Register - 0xF200 0010							
BIT	7	6	5	4	3	2	1	0
Field	CLE	ALE	WP	RSVD	RSVD	RSVD	RSVD	RSVD
OPER	R/W			R				
RESET	0	0	1	0	0	0	0	0

WP	Write Protect. If cleared, WP is not asserted when the device is accessed. If set, WP is asserted when the device is accessed.
ALE	Address Latch Enable. If cleared, ALE is not asserted when the device is accessed. If set, ALE is asserted when the device is accessed.
CLE	Command Latch Enable. If cleared, CLE is not asserted when the device is accessed. If set, CLE is asserted when the device is accessed.
RSVD	Reserved for future implementation.

3.1.9 NAND Flash Chip 1 Select Register

The MVME7100ET provides a Select Register for the NAND Flash device.

Table 3-10 NAND Flash Chip 1 Select Register

REG	NAND Flash Chip 1 Select Register - 0xF200 0011							
BIT	7	6	5	4	3	2	1	0
Field	CE1	CE2	CE3	CE4	RSVD	RSVD	RSVD	RSVD
OPER	R/W				R			
RESET	0	0	0	0	0	0	0	0

CE4	Chip Enable 4. If cleared, CE4 is not asserted when the device is accessed. If set, CE4 is asserted when the device is accessed.
CE3	Chip Enable 3. If cleared, CE3 is not asserted when the device is accessed. If set, CE3 is asserted when the device is accessed.
CE2	Chip Enable 2. If cleared, CE2 is not asserted when the device is accessed. If set, CE2 is asserted when the device is accessed.
CE1	Chip Enable 1. If cleared, CE1 is not asserted when the device is accessed. If set, CE1 is asserted when the device is accessed.
RSVD	Reserved for future implementation.

3.1.10 NAND Flash Chip 1 Presence Register

The MVME7100ET provides a Presence Register for the NAND Flash device.

Table 3-11 NAND Flash Chip 1 Presence Register

REG	**NAND Flash Chip 1 Presence Register - 0xF200 0014**							
BIT	7	6	5	4	3	2	1	0
Field	C1P	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
OPER	R							
RESET	X	0	0	0	0	0	0	0

C1P	Chip 1 Present. If cleared, chip 1 is not installed on the board. If set, chip 1 is installed on the board.
RSVD	Reserved for future implementation.

3.1.11 NAND Flash Chip 1 Status Register

The MVME7100ET provides a Status Register for the NAND Flash device.

Table 3-12 NAND Flash Chip 1 Status Register

REG	NAND Flash Chip 1 Presence Register - 0xF200 00145							
BIT	7	6	5	4	3	2	1	0
Field	RB1	RB2	RB3	RB4	RSVD	RSVD	RSVD	RSVD
OPER	R							
RESET	1	1	1	1	0	0	0	0

RB4	Ready/Busy 4. If cleared, Device 4 is busy. If set, device 4 is ready.
RB3	Ready/Busy 3. If cleared, Device 3 is busy. If set, device 3 is ready.
RB2	Ready/Busy 2. If cleared, Device 2 is busy. If set, device 2 is ready.
RB1	Ready/Busy 1. If cleared, Device 1 is busy. If set, device 1 is ready.
RSVD	Reserved for future implementation.

3.1.12 NAND Flash Chip 2 Control Register

The MVME7100ET provides a Control Register for the NAND Flash device.

Table 3-13 NAND Flash Chip 2 Control Register

REG	NAND Flash Chip 2 Control Register - 0xF200 0018							
BIT	7	6	5	4	3	2	1	0
Field	CLE	ALE	WP	RSVD	RSVD	RSVD	RSVD	RSVD
OPER	R/W			R				
RESET	0	0	1	0	0	0	0	0

WP	Write Protect. If cleared, WP is not asserted when the device is accessed. If set, WP is asserted when the device is accessed.
ALE	Address Latch Enable. If cleared, ALE is not asserted when the device is accessed. If set, ALE is asserted when the device is accessed.
CLE	Command Latch Enable. If cleared, CLE is not asserted when the device is accessed. If set, CLE is asserted when the device is accessed.
RSVD	Reserved for future implementation.

3.1.13 NAND Flash Chip 2 Select Register

The MVME7100ET provides a Select Register for the NAND Flash device.

Table 3-14 NAND Flash Chip 2 Select Register

REG	**NAND Flash Chip 2 Select Register - 0xF200 0019**							
BIT	7	6	5	4	3	2	1	0
Field	CE1	CE2	CE3	CE4	RSVD	RSVD	RSVD	RSVD
OPER	R/W				R			
RESET	0	0	0	0	0	0	0	0

CE4	Chip Enable 4. If cleared, CE4 is not asserted when the device is accessed. If set, CE4 is asserted when the device is accessed.
CE3	Chip Enable 3. If cleared, CE3 is not asserted when the device is accessed. If set, CE3 is asserted when the device is accessed.
CE2	Chip Enable 2. If cleared, CE2 is not asserted when the device is accessed. If set, CE2 is asserted when the device is accessed.
CE1	Chip Enable 1. If cleared, CE1 is not asserted when the device is accessed. If set, CE1 is asserted when the device is accessed.
RSVD	Reserved for future implementation.

3.1.14 NAND Flash Chip 2 Presence Register

The MVME7100ET provides a Presence Register for the NAND Flash device.

Table 3-15 NAND Flash Chip 2 Presence Register

REG	NAND Flash Chip 2 Presence Register - 0xF200 001C							
BIT	7	6	5	4	3	2	1	0
Field	C2P	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
OPER	R							
RESET	X	0	0	0	0	0	0	0

C2P — Chip 2 Present. If cleared, chip 1 is not installed on the board. If set, chip 2 is installed on the board.

RSVD — Reserved for future implementation.

3.1.15 NAND Flash Chip 2 Status Register

The MVME7100ET provides a Status Register for the NAND Flash device.

Table 3-16 NAND Flash Chip 2 Status Register

REG	**NAND Flash Chip 2 Status Register - 0xF200 001D**							
BIT	7	6	5	4	3	2	1	0
Field	RB1	RB2	RB3	RB4	RSVD	RSVD	RSVD	RSVD
OPER	R							
RESET	1	1	1	1	0	0	0	0

RB4 — Ready/Busy 4. If cleared, Device 4 is busy. If set, device 4 is ready.

RB3 — Ready/Busy 3. If cleared, Device 3 is busy. If set, device 3 is ready.

RB2 — Ready/Busy 2. If cleared, Device 2 is busy. If set, device 2 is ready.

RB1 — Ready/Busy 1. If cleared, Device 1 is busy. If set, device 1 is ready.

RSVD — Reserved for future implementation.

3.1.16 Watch Dog Timer Load Register

The MVME7100ET provides a watch dog timer load register.

Table 3-17 Watch dog timer Load Register

REG	**Watch Dog Timer Control Register - 0xF200 0020**							
BIT	7	6	5	4	3	2	1	0
Field	Load							
OPER	R/W							
RESET	0	0	0	0	0	0	0	0

LOAD — Counter Load. When the pattern 0xDB is written, the watch dog counter will be loaded with the count value.

3.1.17 Watch Dog Control Register

The MVME7100ET provides a watch dog timer control register.

Table 3-18 Watch Dog Timer Control Register

REG	**Watch Dog Timer Control Register - 0xF200 0024**							
BIT	7	6	5	4	3	2	1	0
Field	EN	SYS RST	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
OPER	R/W		R					
RESET	0	0	0	0	0	0	0	0

SYSRST — System Reset. If cleared a board-level reset is generated when a time-out occurs. If set, a VMEbus SYSRST is generated when a time-out occurs. If MVME7100ET is SYSCON, then a local reset will also result in a VMEbus SYSRST.

EN — Enable. If cleared the watch dog timer is disabled. If set the watch dog timer is enabled.

RSVD — Reserved for future implementation.

3.1.18 Watch Dog Timer Resolution Register

The MVME7100ET provides a watch dog timer resolution register.

Table 3-19 Watch Dog Timer count Register

REG	Watch Dog Timer Resolution Register - 0xF200 0025							
BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RES			
OPER	R				R/W			
RESET	0	0	0	0	9			

RES	Resolution.	These bits define the resolution of the counter.
	0:	2 µs
	1:	4 µs
	2:	8 µs
	3:	16 µs
	4:	32 µs
	5:	64 µs
	6:	128 µs
	7:	256 µs
	8:	512 µs
	9:	1 µs (default)
	10:	2 µs
	11:	4 µs
	12:	8 µs
	13:	16 µs
	14:	32 µs
	15:	64 µs
RSVD		Reserved for future implementation.

3.1.19 Watch Dog Timer Count Register

The MVME7100ET provides a watch dog timer count register.

Table 3-20 Watch Dog Timer Resolution Register

REG	Watch Dog Timer Counter Register - 0xF200 0026
BIT	15:0
Field	Count
OPER	R/W
RESET	03FF

COUNT — Count. These bits define the watch dog timer count value. When the watch dog counter is enabled or there is a write to the load register, the watch dog counter is set to the count value. When enabled the watch dog counter will decrement at a rate defined by the resolution register. The counter will continue to decrement until it reaches zero or the software writes to the load register. If the counter reaches zero a system or board-level reset will be generated.

3.1.20 PLD Revision Register

The MVME7100ET provides a PLD revision register that can be read by the system software to determine the current revision of the timers/registers PLD.

Table 3-21 PLD Revision Register

REG	PLD Revision Register - 0xF200 0030							
BIT	7	6	5	4	3	2	1	0
Field	PLD_REV							
OPER	R							
RESET	01							

PLD_REV — 8-bit field containing the current timer/register PLD revision. The revision number starts with 01.

3.1.21 PLD Date Code Register

The MVME7100ET PLD provides a 32-bit register which contains the build date code of the inters/registers PLD.

Table 3-22 PLD Date Code Register

REG	**Test Register 1 - 0xF200 0034**			
BIT	31:24	23:16	15:8	7:0
Field	yy	mm	dd	vv
OPER	R			
RESET	xxxx			

yy	Last two digits of year
mm	Month
dd	Day
vv	Version of the day

3.1.22 Test Register 1

The MVME7100ET provides a 32-bit general purpose read/write register which can be used by software for PLD test or general status bit storage.

Table 3-23 Test Register 1

REG	Test Register 1 - 0xF200 0038
BIT	31:0
Field	TEST1
OPER	R/W
RESET	0000

TEST1	General purpose 32-bit R/W field.

3.1.23 Test Register 2

The MVME7100ET provides a second 32-bit test register that reads back the complement of the data in Test Register 1.

Table 3-24 Test Register 2

REG	Test Register 2 - 0xF200 003C
BIT	31:0
Field	TEST2
OPER	R/W
RESET	FFFF

TEST2 A read from this address will return the complement of the data pattern in Test Register 1. A write to this address will write the uncomplemented data to register TEST1.

3.1.24 External Timer Registers

The MVME7100ET provides a set of tick timer registers for access to the four external timers implemented in the timers/registers PLD. Note that these registers are 32-bit registers and are not byte writable. The following sections describe the external timer prescaler and control registers.

3.1.24.1 Prescaler

The Prescaler Adjust value is determined by this formula:

Prescaler Adjust=256-(CLKIN/CLKOUT)

Where CLKIN is the input clock source in MHz and CLKOUT is the desired output clock reference in MHz.

Table 3-25 Prescaler Register

REG	Prescaler Register - 0xF202 0000 (8 bits of a 32-bit register)							
BIT	7	6	5	4	3	2	1	0
Field	Prescaler Adjust							
OPER	R/W							

Table 3-25 Prescaler Register (continued)

REG	**Prescaler Register - 0xF202 0000 (8 bits of a 32-bit register)**
RESET	$E7

The prescaler provides the clock required by each of the four timers. The tick timers require a 1MHz clock input. The input clock to the prescaler is 25MHz. The default value is set for $E7 which gives a 1 MHz reference clock for a 25MHz input clock source.

3.1.24.2 Control Registers

Table 3-26 Tick Timer Control Registers

REG	**Tick Timer 1 Control Register - 0xF202 0010 (32 bits)** **Tick Timer 2 Control Register - 0xF202 0020 (32 bits)** **Tick Timer 3 Control Register - 0xF202 0030 (32 bits)** **Tick Timer 4 Control Register - 0xF202 0040 (32 bits)**												
BIT	31	…	11	10	9	8	7	6	5	4	3	2	1	0
Field	RSVD	…	RSVD	INTS	CINT	ENINT	OVF				RSVD	COVF	COC	ENC
OPER	R/W													
RESET	0	…	0	0	0	0	0	0	0	0	0	0	0	0

ENC — Enable counter. When the bit is set the counter increments
When the bit is cleared the counter does not increment.

COC — Clear Counter on Compare. When the bit is set the counter is reset to 0 when it compares with the compare register.
When the bit is cleared the counter is not reset.

COVF — Clear Overflow Bits. The overflow counter is cleared when a 1 is written to this bit.

OVF — Overflow Bits. These bits are the output of the overflow counter. The overflow counter is incremented each time the tick timer sends an interrupt to the local bus interrupter. The overflow counter can be cleared by writing a 1 to the COVF bit.

ENINT	Enable Interrupt. When the bit is set the interrupt is enabled. When the bit is cleared the interrupt is not enabled.
CINT	Clear Interrupt.
INTS	Interrupt Status.
RSVD	Reserved for future implementation.

3.1.24.3 Compare Register

The tick timer counter is compared to the Compare Register. When they are equal, the tick timer interrupt is asserted and the overflow counter is incremented. If the clear-on-compare mode is enabled the counter is also cleared. For periodic interrupts this equation should be used to calculate the compare register value for a specific period (T):

Compare register value=T (us)

When programming the tick timer for periodic interrupts the counter should be cleared to zero by software and then enabled. If the counter does not initially start at zero, the time to the first interrupt may be longer or shorter than expected. Note that the rollover time for the counter is 71.6 minutes.

Table 3-27 Tick Timer Compare Registers

REG	**Tick Timer 1 Compare Register - 0xF202 0014 (32 bits)** **Tick Timer 2 Compare Register - 0xF202 0024 (32 bits)** **Tick Timer 3 Compare Register - 0xF202 0034 (32 bits)** **Tick Timer 4 Compare Register - 0xF202 0044 (32 bits)**		
BIT	31	…	0
Field	Tick Timer Compare Value		
OPER	R/W		
RESET	0		

3.1.24.4 Counter Register

When enabled the tick timer counter register increments every microsecond. software may read or write the counter at any time.

Table 3-28 Tick Timer Counter Register

REG	Tick Timer 1 Counter Register - 0xF202 0018 (32 bits) Tick Timer 2 Counter Register - 0xF202 0028 (32 bits) Tick Timer 3 Counter Register - 0xF202 0038 (32 bits) Tick Timer 4 Counter Register - 0xF202 0048 (32 bits)		
BIT	31	…	0
Field	Tick Timer Counter Value		
OPER	R/W		
RESET	0		

3.1.25 Geographical Address Register

The VMEbus Status Register in the Tsi148 provides the VMEbus geographical address of the MVME7100ET. This register reflects the inverted states of the geographical address pins at the 5-row, 160-pin P1 connector. Applications not using the 5-row backplane can use the planar switch described in the MVME7100ET Installation and Use manual to assign a geographical address.

Programming Details

4.1 Overview

This chapter includes additional programming information for the MVME7100ET.

4.2 MC864xD Reset Configuration

The MVME7100ET supports the power-on reset (POR) pin sampling method for processor reset configuration. The states of the various configuration pins on the processor are sampled when reset is deasserted to determine the desired operating modes. Combinations of pull-up and pull-down resistors are used to set the options. Some options are fixed and some are selectable at build time by installing the proper pull-up/pull-down resistor. Each option and the corresponding default setting are described in the following table. Refer to the MC864xD reference manual, listed in *Appendix B, Related Documentation on page 79* and *Manufacturers' Documents on page 79* for additional details and/or programming information.

Table 4-1 MC864xD POR Configuration Settings

MC864xD Signal	Select Option	Default POR Settings	Description	State of Bit vs Function1	
LA [28:31]	Resistors	1000	MPX Clock PLL Ratio (MPX Clock: SYSCLK)	0000	16:1
				0010	2:1
				0011	3:1
				0100	4:1
				0101	5:1
				0110	6:1
				1000	8:1
				1001	9:1
TSEC1_TXD[1]	Resistors	1	Platform Frequency	0	Platform frequency of 400 MHz
				1	Platform frequency of 500MHz or greater

Table 4-1 MC864xD POR Configuration Settings (continued)

MC864xD Signal	Select Option	Default POR Settings	Description	State of Bit vs Function1	
LDP[0:3], LA[27]	Resistors	0_1100 for the 1.3GHz processor 0_1000 for the 1.067GHz processor	(e600 Core: MPX Clock)	0_1000	2:1
				0_1100	2.5:1
				1_0000	3:1
				1_1100	3.5:1
				1_0100	4:1
				0_1110	4.5:1
TSEC3_TXD[2]	Resistor	1 (no option for disabled)	Core 1 Enable	0	Core 1 disabled
				1	Core 1 enabled
TSEC3_TXD[3]	Switch	1	Core 1 Low Memory offset	0	Real address A in range 0 to 256MB-1 translated to Address A + 256MB
				1	sys addr = real addr
TSEC2_TXD[0:3	Resistors	1111(no option for pulldowns)	Boot ROM location	0000	PCI Express 1
				0001	PCI Express 2
				0010	Serial RapidIO
				0100	DDR Memory Controller 1
				0101	DDR Memory Controller 2
				1101	Local Bus GPCM - 8-bit ROM
				1110	Local Bus GPCM - 16
				1111	Local Bus GPCM -32 -bit ROM
TSEC1_TXD[0]	Resistor	1 (no option pulldown)	Alternate Boot Vector Location	0	PCI-E 1 outbound ATMU window 1 is enabled
				1	Boot vector fetched from default boot ROM location

Table 4-1 MC864xD POR Configuration Settings (continued)

MC864xD Signal	Select Option	Default POR Settings	Description	State of Bit vs Function1	
TSEC4_TXD[0:3]	Resistors	1111 (no options for pulldowns)	I/O Port Selection	0010	SerDes1: x1/x2/x4/x8 PCIE, 100 MHz ref clkSerDes2: disabled
				0011	SerDes1: x1/x2/x4/x8 PCIE, 100 MHz ref clk SerDes2: x1/x2/x4/x8 PCIE, 100 MHz ref clk
				0101	SerDes1: x1/x2/x4/x8 PCIE, 100 MHz ref clk SerDes2: x4 Serial RapidIO
				0110	SerDes1: x1/x2/x4/x8 PCIE, 100 MHz ref clk SerDes2: x4 Serial RapidIO
				0111	SerDes1: x1/x2/x4/x8 PCIE, 100 MHz ref clk SerDes2: x4 Serial RapidIO
				1001	SerDes1: disabled SerDes2: x4 Serial RapidIO
				1010	SerDes1: disabled SerDes2: x4 Serial RapidIO
				1011	SerDes1: disabled SerDes2: x4 Serial RapidIO
				1110	SerDes1: disabled SerDes2: x1/x2/x4/x8 PCIE
				1111	SerDes1: x1/x2/x4/x8 PCI-E, 100 MHz ref clk SerDes2: x1/x2/x4/x8 PCI-E, 100 MHz ref clk

Table 4-1 MC864xD POR Configuration Settings (continued)

MC864xD Signal	Select Option	Default POR Settings	Description	State of Bit vs Function1	
LWE[2:3]	Control PLD	11	Host/Agent Config	00	SerDesn port is PCIE, then it is an endpoint. SerDes2 port is SRIO, then it is an agent.
				01	SerDes1 port is PCIE, then it is a root complex. SerDes2 port is PCIE, then it is an endpoint. SerDes2 port is SRIO, then it is an host.
				10	SerDes1 port is PCIE, then it is an endpoint. SerDes2 port is PCIE, then it is a root complex. SerDes2 part is SRIO, then it is an agent.
				11	SerDesn port is PCIE, then it is a root complex. SerDes2 part is SRIO, then it is a host.
LWE[0]	Control PLD	1	CPU Boot Configuration	0	CPU boot holdoff mode.
				1	The core 0 is allowed to boot without waiting for configuration by an external master
LGPL3, LGPL5	Testpoints	11	Boot Sequencer Configuration	01	Normal I2C addressing
				10	Extended I2C addressing
				11	Boot sequencer is disabled
TSEC2_TXD[4] TSEC2_TX_ER	No Connects	11 (default)	DDR SDRAM Type	01	DDR1
				11	DDR2

Table 4-1 MC864xD POR Configuration Settings (continued)

MC864xD Signal	Select Option	Default POR Settings	Description	State of Bit vs Function1	
TSECn_TXD5	Resistors	0 (pulldowns)	eTSEC Width Configuration	0	Ethernet interface operates in reduced mode, RTBI or RGMII.
				1	Ethernet interface operates in standard TBI or GMII modes.
TSECn_TXD[6:7]	Resistor	10	eTSECn Protocol Configuration	00	eTSECn controller operates using FIFO.
				01	eTSECn controller operates using MII(RMII).
				10	eTSECn controller operates using GMII(RGMII)
				11	eTSECn controller operates using TBI
TSEC1_TXD[2:4]	Processor Default	111	RapidIO Device ID	Device ID used for serial RapidIO hosts.	
LWE1	Control PLD	1	Serial RapidIO System Size	0	Up to 65,536 devices
				1	Up to 256 devices
D1_MSRCID[0]	No Connect	1 (processor default)	Memory Debug Configuration	0	Debug information from LBC is driven on the D1_MSRCIDn and D1_MDVAL signals
				1	Debug information from DDR SDRAM controller is driven on the D1_MSRCID and D1_MDVAL signals
D1_MSRCID[1]	No Connect	1 (processor default)	DDR Debug Configuration	0	DDR debug information is driven on the ECC pins instead of the normal ECC I/O.
				1	DDR debug information is not driven on the ECC pins.

4.3 MC864xD Interrupt Controller

The MVME7100ET uses the MC864xD integrated programmable interrupt controller (PIC) to manage locally generated interrupts. Currently defined external interrupting devices and interrupt assignments, along with corresponding edge/levels and polarities, are shown in the following table.

Table 4-2 MC864xD Interrupt Controller

Interrupt #	Edge/Level	Polarity	Interrupt Source	Notes
0	Level	Low	PCI Express Port 1	
1	Level	Low	PCI Express Port 1	
2	Level	Low	PCI Express Port 1	
3	Level	Low	PCI Express Port 1	
4	Level	Low	PCI Express Port 2	
5	Level	Low	PCI Express Port 2	
6	Level	Low	PCI Express Port 2	
7	Level	Low	PCI Express Port 2	
8	Level	Low	XMCspan	
9	Level	Low	RTC, TEMP, Abort	
10	Level	Low	PHYs	
11	Level	Low	UARTs, External Timer	1,2

NOTES:

1. External timers are implemented in a PLD.
2. External UARTs are implemented using a QUART.
3. Refer to the *MC864xD Reference Manual* listed in *Related Documentation on page 79*, for additional details regarding the operation of the MC864xD PIC.

4.4 Local Bus Controller Chip Select Assignments

The following table shows local bus controller (LBC) bank and chip select assignments for the MVME7100ET board.

Table 4-3 LBC Chip Select Assignments

LBC Bank / Chip Select	Local Bus Function	Size	Data Bus Width	Notes
0	Boot flash bank	128MB	32 bits	1
1	Boot flash bank	128MB	32 bits	1
2	NAND flash bank	64KB	8 bits	
3	MRAM	512KB	16 bits	4
4	Control/status registers	64KB	32 bits	2
5	Quad UART	64KB	8 bits	
6	32-bit Timers	64KB	32 bits	3
7	Not Used			

NOTES:

1. Flash bank size determined by VPD flash packet.
2. Control/Status registers are byte read and write capable.
3. 32-bit timer registers are byte readable, but must be written as 32 bits.

4.5 I^2C Device Addresses

A two-wire serial interface is provided by an I^2C compatible serial controller integrated into the MC864xD. The MC864xD I^2C controller is used by the system software to read the contents of the various I^2C devices located on the MVME7100ET. The following table contains the I^2C devices used for the MVME7100ET and their assigned device addresses.

Table 4-4 I2C Bus Device Addressing

I2C Bus Address	Device Address A2 A1 A0 (binary)	Size (bytes)	Device Function	Notes
$98	N/A	N/A	ADT7461 temperature sensor	

Table 4-4 I2C Bus Device Addressing (continued)

I2C Bus Address	Device Address A2 A1 A0 (binary)	Size (bytes)	Device Function	Notes
$A0	000	256 x 8	DDR2 memory bank 1 SPD	1
$A2	001	256 x 8	DDR2 memory bank 2 SPD	1
$A4	010	65,536 x 8	User configuration	2
$A6	011	65,536 x 8	User configuration	2
$A8	100	8192 x 8	VPD (on-board system configuration)	2
$AA	101	8192 x 8	RTM VPD (off-board configuration)	2, 3
$AC	110		Reserved	
$AE	111		Reserved	
$D0	N/A	N/A	DS1375 real-time clock	

NOTES:

1. Each SPD defines the physical attributes of each bank or group of banks.
2. This is a dual address serial EEPROM.
3. The device address is user selectable using switches on the RTM. The recommended address setting for the ADT7461 is $AA.

4.6 User Configuration EEPROM

The board provides two 64KB dual address serial EEPROMs for a total of 128KB user configuration storage. These EEPROMs are hardwired to have device IDs as shown in *Table 4-4 on page 49*, and each device ID will not be used for any other function. Refer to the *EEPROM Datasheet* listed in *Appendix B, Related Documentation*, for additional details.

4.7 VPD EEPRO

The MVME7100ET board provides an 8KB dual address serial EEPROM containing Vital Product Data (VPD) configuration information specific to the MVME7100ET. Typical information that may be present in the EEPROM may include: manufacturer, board revision, build version, date of assembly, memory present, options present, L2 cache information, and so on. The VPD EEPROM is hardwired to have a device ID as shown in *Table 4-4 on page 49*. Refer to the *EEPROM Datasheet* listed in *Appendix B, Related Documentation*, for additional details.

4.8 RTM VPD EEPROM

The MVME7100ET RTM provides an 8 KB dual address serial EEPROM containing VPD configuration information specific to the MVME7100ET RTM. Typical information that may be present in the EEPROM may include: manufacturer, board revision, build version, date of assembly, options present, and so on. The RTM VPD EEPROM device ID is user selectable with the recommended value for MVME7100ET as shown in *Table 4-4 on page 49*. Refer to the *EEPROM Datasheet* listed in *Appendix B, Related Documentation*, for additional details.

4.9 Ethernet PHY Address

The assigned Ethernet PHY addresses on the MC864xD MII management (MIIM) bus is shown in the following table. Need new table data.

Table 4-5 PHY Types and MII Management Bus Addresses

MC864xD Ethernet Port	Function/Location	PHY Types	PHY MIIM Address [4:0]
TSEC1	Gigabit Ethernet port 1 routed to front panel	BCM5482SH	01
TSEC2	Gigabit Ethernet port 2 routed to front panel	BCM5482SH	02
TSEC3	Gigabit Ethernet port routed to P2	BCM5482SH	03
TSEC4	Gigabit Ethernet port routed to P2	BCM5482SH	04

4.10 Flash Memory

The MVME7100ET is designed to provide 128MB of soldered-on NOR flash memory. Two AMD +3.0V devices are configured to operate in 16-bit mode to form a 32-bit flash bank. This flash bank is also the boot bank and is connected to LBC Chip Select 0 and 1. The NOR flash is accessed via the MC864xD local bus. The table below shows memory size and device IDs.

Table 4-6 NOR Flash Memory Configurations

Device Part Number	Data Bus Width	Bank Size	Device Size	Vendor ID	Device ID
S29GL512N10	32 bits	128 MB	512 megabit	AMD-0001h	7E23h

A hardware Flash Bank write-protect switch is provided on the MVME7100ET to enable write protection of the NOR flash. Regardless of the state of the software flash write-protect bit in the NOR Flash Control/Status register, write protection is enabled when this switch is ON. When the switch is OFF, write protection is controlled by the state of the software flash write-protect bits. It is only disabled by clearing this bit in the NOR Flash Control/Status register (refer to section 4.1.6.4). Note that the F_WE_HW bit reflects the state of the switch and is only software readable whereas the F_WP_SW bit supports both read and write operations.

Also included is one bank of NAND flash which is accessed via the MC864xD local bus. The table below shows the memory sizes and device IDs.

Table 4-7 NAND Flash Memory Configurations

Device Part Number	Data Bus Width	Bank Size	Device Size	Vendor ID	Device ID
K9LBG08U0M	8 bits	4 GB	4 GB	Samsung = ECh	D7h
K9HCG08U1M	8 bits	4 GB	8 GB	Samsung = ECh	D7h

4.11 PCI/PCI-X Configuration

The sections below provide information that details the PCI/PCI-X configuration of the various on-board PCI devices.

4.11.1 PCI IDSEL and Interrupt Definition

Each PCI device has an associated address line connected via a resistor to its IDSEL pin for Configuration Space accesses. The following table shows the IDSEL assignments for the PCI devices and slots on each of the PCI busses on the board along with the corresponding interrupt assignment to the PIC external interrupt pins. Refer to the MC864xD datasheet and the PEX8114, PEX8112 and PEX8525 data sheets for details on generating configuration cycles on each of the PCI busses.

Table 4-8 IDSEL and Interrupt Mapping for PCI Devices

Device Number Field	PCI Bus	AD Line for IDSEL	PCI Device or Slot	Device/Slot INT to MC864xD IRQ			
				INTA#	INTB#	INTC#	INTD#
A (8641D)	0b0_0000	internal	MC864xD				

Table 4-8 IDSEL and Interrupt Mapping for PCI Devices (continued)

Device Number Field	PCI Bus	AD Line for IDSEL	PCI Device or Slot	Device/Slot INT to MC864xD IRQ			
				INTA#	**INTB#**	**INTC#**	**INTD#**
PCI1 (PEX8114)	0b0_0100	20	PMC1 Primary	INTA IRQ1	INTB IRQ2	INTC IRQ3	INTD IRQ0
	0b0_0101	21	PMC1 Secondary	INTB IRQ2	INTC IRQ3	INTD IRQ0	INTA IRQ1
PCI2 (PEX8114)	0b0_0100	20	PMC2 Primary	INTA IRQ2	INTB IRQ3	INTC IRQ0	INTD IRQ1
	0b0_0101	21	PMC2 Secondary	INTB IRQ3	INTC IRQ0	INTD IRQ1	INTA IRQ2
PCI3 (PEX8114)	0b0_0010	18	Tsi148 VME	INTC IRQ3	INTD IRQ0	INTA IRQ1	INTB IRQ2
PCI4 (PEX8112)	0b0_0010	18	uPD720101 USB	INTC IRQ3	NC IRQ0	INTA IRQ1	INTB IRQ2

Refer to the MC864xD reference manual for additional details about the MC864xD PIC operation.

The following table shows the Vendor ID and the Device ID for each of the planar PCI devices on the MVME7100ET.

Table 4-9 Planar PCI Device Identification

Function	Device	Vendor ID	Device ID
System Controller	MC864xD	0x1957	0x7011
PCI-E Switch	PEX8525	0x10B5	0x8525
PCI-E-to-PCI Bridge	PEX8112	0x10B5	0x8112
PCI-E-to-PCI-X Bridge	PEX8114	0x10B5	0x8114
VME Controller	TSi148	0x10E3	0x0148

4.11.2 PCI Arbitration Assignments

The integrated PCI/X arbiters internal to the PEX8112 and the PEX8114 provide PCI arbitration for the MVME7100ET.

The arbitration assignments on the MVME7100ET are shown in the table below so that software may set arbiter priority assignments if necessary.

Table 4-10 PCI Arbitration Assignments

PCI Bus	Arbitration Assignment	PCI Master(s)
1	PEX8114 REQ/GNT[0]	PMC site 1 primary master
1	PEX8114 REQ/GNT[1]	PMC site 1 secondary master
2	PEX8114 REQ/GNT[0]	PMC site 2 primary master
2	PEX8114 REQ/GNT[1]	PMC site 2 secondary master
3	PEX8114 REQ/GNT[0]	Tsi148 VME Controller

4.12 Other Software Considerations

4.12.1 LBC Timing Parameters

The following table defines the timing parameters for the devices on the local bus.

Table 4-11 LBC Timing Parameters

	0 NOR Flash	1 NOR Flash	2 NAND Flash	3 MRAM	4 CSR	5 UART	6 Timers
BCTLD	0	0	0	0	0	0	0
CSNT	1	1	1	1	0	1	0
ACS	3	3	0	0	0	0	0
XACS	1	1	0	0	0	0	0
SCY	4	4	3	1	5	2	5
SETA	0	0	0	0	0	0	0
TRLX	0	0	1	1	0	1	0

Table 4-11 LBC Timing Parameters (continued)

	0 NOR Flash	1 NOR Flash	2 NAND Flash	3 MRAM	4 CSR	5 UART	6 Timers
EHTR	0	0	0	0	0	0	0
EAD	0	0	0	0	0	0	0

4.13 Clock Distribution

The clock function generates and distributes all the clocks required for system operation. The PCI-E clocks are generated using an eight output differential clock driver. The PCI/PCI-X bus clocks are generated by the bridge chips from the PCI-E clock. Additional clocks required by individual devices are generated near the devices using individual oscillators. The following table lists the clocks required on the MVME7100ET along with their frequency and source.

Table 4-12 Clock Assignments

Device	Clock Signals	Frequency (MHz)	Clock Tree Source	Qty	VIO
CLK_CPU	MC864xD	66	Oscillator	1	+3.3 V
MC864xD	CLK125MHZ	125	Oscillator	1	+2.5 V
MC864xD	CLK_RTC	1	PLD	1	+3.3 V
PMC1	CLK_PCI1	33/66/100	PEX8114	1	+3.3 V
PMC2	CLK_PCI2	33/66/100	PEX8114	1	+3.3 V
Tsi148	CLK_PCI3	133	PEX8114	1	+3.3 V
USB	CLK_PCI4	33	PEX8112	1	+3.3 V
BCM5482S	CLK2_25MHZ	25	Oscillator/Buffer	1	+2.5 V
BCM5482S	CLK3_25MHZ	25	Oscillator/Buffer	1	+2.5 V
Control and Timers PLD	CLK1_25MHZ CLK_LBP	25 MPX CLK / 8	Oscillator/Buffer MC864xD	1 1	+3.3 V +3.3 V
QUART	CLK_1.8M	1.8432	Oscillator	1	+3.3 V

Table 4-12 Clock Assignments (continued)

Device	Clock Signals	Frequency (MHz)	Clock Tree Source	Qty	VIO
RTC	CLK_32K	32.768 KHz	Crystal	1	+3.3 V
ICS9FG108	CLK4_25MHZ	25	Oscillator	1	+3.3 V
PEX8525	CLK_PCIE0	100	ICS9FG108	1	DIFF
PEX8114	CLK_PCIE1	100	ICS9FG108	1	DIFF
PEX8114	CLK_PCIE2	100	ICS9FG108	1	DIFF
PEX8114	CLK_PCIE3	100	ICS9FG108	1	DIFF
PEX8112	CLK_PCIE4	100	ICS9FG108	1	DIFF
MC864xD	CLK_PCIE5	100	ICS9FG108	1	DIFF
MC864xD	CLK_PCIE6	100	ICS9FG108	1	DIFF
XMCspan	CLK_PCIE7	100	ICS9FG108	1	DIFF

4.13.1 System Clock

The system clock is driven by an oscillator. The following table defines the clock frequencies for various configurations.

Table 4-13 Clock Frequencies

SYSCLK	Core	MXP (Platform)	DDR2
66.67MHz	1.3GHz	533MHz	266MHz
66.67MHz	1.067GHz	533MHz	266MHz

4.13.2 Real Time Clock Input

The RTC clock input is driven by 1MHz clock generated by the Control and Timers PLD. This provides a fixed clock reference for the MC864xD PIC timers, which software can use as a known timing reference.

4.13.3 Local Bus Controller Clock Divisor

The Local Bus Controller (LBC) clock output is connected to the PLD but is not used by the internal logic.

Programmable Configuration Data

A.1 Overview

This appendix provides data and specifications pertaining to programmable parts used on the MVME7100ET. The board is shipped after the programmable parts have been programmed through ATE or boundary scan according to the In-Circuit Test specifications.

Table A-1 Programmable Devices

Location	Raw Part #	Manufacturer Part #	Specification Data File	Description
U49	51NL9637X71	AT24C64CN-TH-T	VPD Contents	MVME7100ET VPD
U50	51NL9637W48	AT24C02BN-SH	SPD Contents	MVME7100ET SPD
U51	51NL9637W48	AT24C02BN-SH	SPD Contents	MVME7100ET SPD

A.2 List of Devices

Several serial EEPROMs with I^2C interfaces exist on the board to store information needed by software to properly configure the board upon start up. The types of configuration data are:

- Vital Product Data (VPD) pertaining to all board functions - only one on the board
- Vital Product Data (VPD) for the RTM
- Serial Presence Detect (SPD) pertaining to SDRAM characteristics - one per bank
- EEPROMs for configuration data storage

The following table lists the on-board and transition module serial EEPROMs.

Table A-2 On-board Serial EEPROMs

Master	Device Function	Size	Device Address (A2A1A0)	I2C Addr.	Notes
I2C1	DRAM SPD	256	000b	$A0	
I2C1	DRAM SPD	256	001b	$A2	
I2C1	User defined	65536	010b	$A4	
I2C1	User defined	65536	011b	$A6	
I2C1	VPD and GEV	8192	100b	$A8	
I2C1	RTM VPD	8192	101b	$AA	

Table A-2 On-board Serial EEPROMs (continued)

Master	Device Function	Size	Device Address (A2A1A0)	I2C Addr.	Notes
I2C1	XMCspan VPD	8192	110b	$AC	

A.3 Vital Product Data (VPD) Introduction

The data listed in the following tables are for general reference information. The VPD identifies board information that may be useful during board initialization, configuration, and verification. This section includes information on how to perform various tasks to read, modify, and correct Vital Product Data, as well as specific format and content information for this product. Information that is contained in the VPD includes:

- Marketing Product Number (xxx)
- Factory Assembly Number (0106839Dxx)
- Serial number of the specific MVME7100ET
- Processor family number (xxx)
- Hardware clock frequencies (internal, external, fixed, PCI bus)
- Component configuration information (connectors, Ethernet, addresses, flash bank ID, L2 cache ID)
- Security information (VPD type, version and revision data, 32-bit CRC protection)

A.4 How to Read and Modify VPD Information

`vpdDisplay` may be used to display VPD information.

`vpdEdit` can be used to modify the VPD information.

A.5 What Happens if VPD Information is Corrupted

If the VPD information becomes corrupted, the following occurs:

- A warning message is displayed in the startup banner.
- The firmware ignores the VPD contents and attempts to acquire information from other sources.
- Some device drivers will not work.
- Some diagnostic tests will fail.
- The board will run much slower than usual.

A.6 How to Fix Corrupted VPD Information

If you encounter corrupted VPD information, use the following method to fix the corrupted data:

- The firmware is designed to reach the prompt with bad VPD.
- Use the **`vpdEdit`** command to fix the VPD.

A.7 What if Your Board Has the Wrong VPD

If your board has the wrong VPD information, the following occurs:

- No warning message is displayed.
- Incorrect VPD information is seen as correct by the firmware.
- The board may hang during startup (no-start condition).
- The board may be very unstable if it reaches the prompt.
- Device drivers, diagnostic tests, and firmware commands may hang or fail in unexpected ways.

A.8 How to Fix Wrong VPD Problems

If you suspect that your board has problems, as a result of wrong VPD information, select SAFE mode by setting S1:1 ON and reboot the MVME7100ET. At this point, the firmware will ignore all EEPROM contents. Use the vpdEdit command to change the VPD to the correct parameters.

A.9 Checksum Guidelines

The next sections provide examples of CRC calculation and SPD checksum calculations.

A.9.1 Vital Product Data CRC Calculation

When computing the CRC this field (for example, 4 bytes) is set to zero. The CRC only covers the range as specified in the size field (4-bytes). Integer values are formatted/stored in big-endian byte ordering. The VPD CRC generation code is shown in the following example.

```
/*
* vpdGenerateCRC - generate CRC data for the passed buffer
* description:
```

```
* This function's purpose is to generate the CRC for the
* passed VPD SROM buffer.
* call:
* argument #1 = buffer pointer
* argument #2 = number of elements
* return:
* CRC data
*/
unsigned int
vpdGenerateCRC(pVpdBuffer, vpdSromSize)
unsigned char *pVpdBuffer;
unsigned int vpdSromSize;
{
unsigned int crcValue;
unsigned int crcValueFlipped;
unsigned char dataByte;
unsigned int index, dataBitValue, msbDataBitValue;
crcValue = 0xffffffff;
for (index = 0; index < vpdSromSize; index++)
{
dataByte = *pVpdBuffer++;
for (dataBitValue = 0; dataBitValue < 8; dataBitValue++)
{
msbDataBitValue = (crcValue >> 31) & 1;
crcValue <<= 1;
if (msbDataBitValue ^ (dataByte & 1))
{
crcValue ^= 0x04c11db6;
crcValue |= 1;
}
dataByte >>= 1;
}
}
crcValueFlipped = 0;
for (index = 0; index < 32; index++)
{
```

```
crcValueFlipped <<= 1;
dataBitValue = crcValue & 1;
crcValue >>= 1;
crcValueFlipped += dataBitValue;
}
crcValue = crcValueFlipped ^ 0xffffffff;
return (crcValue);
}
```

A.9.2 Serial Presence Detect Checksum Calculation

The calculation process is as follows:

1. Convert binary information, in byte locations 0 - 62, to decimal.
2. Add together (sum) all decimal values for addresses 0 - 62.
3. Divide sum by 256.
4. Convert remainder to binary (will be less than 256).
5. Store result (single byte) in address 63 as “Checksum”.

The same result can be obtained by adding the binary values in addresses 0 - 62 and eliminating all but the low order byte. The low order byte is the “Checksum”.

Table A-3 Checksum Calculation Example

SPD Byte Address	Serial PD		Convert to Decimal
00 (0x00)	0010 0100	>	36
01 (0x01)	1111 1110	>	+ 254
02 (0x02)	0000 0000	>	+ 0
03 (0x03)	0000 0000	>	+ 0
:	:	>	+ 0
:	:	>	
60 (0x3C)	0000 0000	>	+ 0
61 (0x3D)	0000 0000	>	+ 0
62 (0x3E)	0000 0000	>	+ 0
Decimal Total	-	-	290

Table A-3 Checksum Calculation Example (continued)

SPD Byte Address	Serial PD		Convert to Decimal
Divide by 256	-	-	1
Remainder	-	-	34
Convert to binary	0010 0010	<	34
63(0x3F)(Checksum)	0010 0010	-	

A.10 VPD Contents for MVME7100ET Boards

The following tables describe the VPD data to be programmed into U49. *Table A-4* contains only the static VPD data and Table A-5 on page 71 contains only the variable VPD data. This information is subject to change (under authority of an engineering change order). If a difference is noted between either of these tables and your board, contact your support representative to determine which is accurate.

Table A-4 Static VPD Contents

Offset (HEX)	Data (HEX)	Field Type	Description
00	45	ASCII	Eye-Catcher ("Penguin Solutions") Note: Lowest CRC byte for the calculation of CRC.
01	4D		
02	45		
03	52		
04	53		
05	4F		
06	4E		
07	20		
08	02	BINARY	Size of VPD area in bytes. The size is viewed as logical; it is not the size of the EEPROM. 512 bytes in this VPD architecture
09	00		
0A	0F	BINARY	VPD Revision Packet
0B	04	BINARY	# of Bytes
0C	00	BINARY	Board Type: Processor Board
0D	03	BINARY	Architecture Revision

Table A-4 Static VPD Contents (continued)

Offset (HEX)	Data (HEX)	Field Type	Description
0E	00	BINARY	Board Build Revision
0F	00	BINARY	Revision Reason Flags
10	01	BINARY	Product Identifier Packet. Refer to Notes 1 and 2.
11	14	BINARY	# of bytes
12	xx	ASCII	Product Identifier. Refer to *Table A-5*.
13	xx		
14	xx		
15	xx		
16	xx		
17	xx		
18	xx		
19	xx		
1A	xx		
1B	xx		
1C	xx		
1D	xx		
1E	xx		
1F	xx		
20	xx		
21	xx		
22	xx		
23	xx		
24	xx		
25	xx		

Table A-4 Static VPD Contents (continued)

Offset (HEX)	Data (HEX)	Field Type	Description
26	02	BINARY	Factory Assembly Number. Refer to Notes 1 and 2.
27	0D	BINARY	# of bytes
28	xx	ASCII	Factory Assembly Number. Refer to *Table A-5* and *Table A-6*.
29	xx		
2A	xx		
2B	xx		
2C	xx		
2D	xx		
2E	xx		
2F	xx		
30	xx		
31	xx		
32	xx		
33	xx		
34	xx		
35	03	BINARY	**Serial number to be filled in. Refer to Notes 2 and 3.
36	07	BINARY	# of bytes
37	xx	ASCII	Most significant serial number character
38	xx		
39	xx		
3A	xx		
3B	xx		
3C	xx		
3D	xx		Least significant serial number character

Table A-4 Static VPD Contents (continued)

Offset (HEX)	Data (HEX)	Field Type	Description
3E	06	BINARY	External Processor Clock Frequency Packet
3F	05	BINARY	# of bytes
40	03	BINARY	Four bytes containing the SYSCLK frequency. 0x03F940AA = 66.66 MHz
41	F9		
42	40		
43	AA		
44	01	BINARY	First Processor
45	08	BINARY	Ethernet MAC Address Packet
46	07	BINARY	# of bytes
47	xx	BINARY	Six bytes containing the lowest Ethernet address.
48	xx		
49	xx		
4A	xx		
4B	xx		
4C	xx		
4D	00	BINARY	Ethernet Controller 0
4E	08	BINARY	Ethernet MAC Address Packet
4F	07	BINARY	# of bytes
50	xx	BINARY	Six bytes containing the next Ethernet address.
51	xx		
52	xx		
53	xx		
54	xx		
55	xx		
56	01	BINARY	Ethernet Controller 1

Table A-4 Static VPD Contents (continued)

Offset (HEX)	Data (HEX)	Field Type	Description
57	08	BINARY	Ethernet MAC Address Packet
58	07	BINARY	# of bytes
59	xx	BINARY	Six bytes containing the next Ethernet address.
5A	xx		
5B	xx		
5C	xx		
5D	xx		
5E	xx		
5F	02	BINARY	Ethernet Controller 2
60	08	BINARY	Ethernet MAC Address Packet
61	07	BINARY	# of bytes
62	xx	BINARY	Six bytes containing the highest Ethernet address.
63	xx		
64	xx		
65	xx		
66	xx		
67	xx		
68	03	BINARY	Ethernet Controller 3
69	09	BINARY	Processor Identifier Packet
6A	05	BINARY	# of bytes
6B	xx	ASCII	Processor type Refer to *Table A-5*.
6C	xx		
6D	xx		
6E	xx		
6F	xx		

Table A-4 Static VPD Contents (continued)

Offset (HEX)	Data (HEX)	Field Type	Description
70	0A	BINARY	EPROM CRC When computing the CRC this field (4 bytes) is set to zero. This CRC only covers the range as Integer (4-byte). Refer to *Vital Product Data CRC Calculation on page 61*. Note: Lower CRC byte for the calculation of CRC = 0x00 Upper CRC byte for the calculation of CRC = 0x1FF
71	04	BINARY	# of bytes
72	xx	BINARY	** CRC to be filled in
73	xx		
74	xx		
75	xx		
76	0B	BINARY	Bank 1 Flash Memory Configuration Packet
77	0C	BINARY	# of bytes
78	00	BINARY	Vendor Identifier
79	01		
7A	7E	BINARY	Device Identifier
7B	23		
7C	10	BINARY	Single device width in bits
7D	02	BINARY	Number of devices or sockets present
7E	01	BINARY	Number of interleave columns
7F	20	BINARY	Column width in bits
80	20	BINARY	Minimum write/erase data width in bits
81	01	BINARY	Flash bank number
82	6E	BINARY	Flash access speed in nanoseconds: 0x6E = 110 ns
83	09	BINARY	Total bank size [(1<<n)*256K bytes]: 0x09 = 128 MB
84	0B	BINARY	Bank 2 Flash Memory Configuration Packet

Table A-4 Static VPD Contents (continued)

Offset (HEX)	Data (HEX)	Field Type	Description
85	0C	BINARY	# of bytes
86	00	BINARY	Vendor Identifier
87	EC		
88	D5	BINARY	Device Identifier
89	51		
8A	08	BINARY	Single device width in bits
8B	xx	BINARY	Number of devices or sockets present: 0x02 for MVME7100-0171ETR and MVME7100-0173ETR. 0x01 for all other assemblies.
8C	01	BINARY	Number of interleave columns
8D	08	BINARY	Column width in bits
8E	08	BINARY	Minimum write/erase data width in bits
8F	02	BINARY	Flash bank number
90	2D	BINARY	Flash access speed in nanoseconds: 0x2D = 45 ns
91	xx	BINARY	Total bank size [(1<<n)*256K bytes]: 0x0E = 4 GB, 0x0F = 8 GB. Refer to *Table A-5*.
92	FF	BINARY	Not Used
:	:	:	:
1FF	FF	BINARY	Not Used

NOTES: Notes

1. This data is not static. Each board must be assigned with an entity unique to the board assembly number.
2. The method used to program the Product Identifier, Factory Assembly Number, and Serial Number packets requires that these packets be located in absolute fixed locations. For this reason, these packets shall have fixed sizes and shall immediately follow the header.

3. This data is not static. Each board's Serial Number packet must be unique. The board's serial number is obtained from the onboard serial number label.

The "xx" in *Table A-5* at address 0x32 represents the assembly revision letter (A=41, B=42, and so on).

Table A-5 Variable VPD Contents

Offset (Hex)	**MVME7100ET-161**	**MVME7100ET-163**	**MVME7100ET-171**	**MVME7100ET-173**
	0106839D11*	**0106839D12***	**0106839D13***	**0106839D14***
	Product Identifier (ASCII)			
12	4D	4D	4D	4D
13	56	56	56	56
14	4D	4D	4D	4D
15	45	45	45	45
16	37	37	37	37
17	31	31	31	31
18	30	30	30	30
19	30	30	30	30
1A	45	45	45	45
1B	54	54	54	54
1C	2D	2D	2D	2D
1D	31	31	31	31
1E	36	36	37	37
1F	31	33	31	33
20	20	20	20	20
21	20	20	20	20
22	20	20	20	20
23	20	20	20	20
24	20	20	20	20
25	20	20	20	20

Table A-5 Variable VPD Contents (continued)

Offset (Hex)	MVME7100ET-161	MVME7100ET-163	MVME7100ET-171	MVME7100ET-173
	0106839D11*	**0106839D12***	**0106839D13***	**0106839D14***
	Factory Assembly Number (ASCII)			
28	30	30	30	30
29	31	31	31	31
2A	30	30	30	30
2B	36	36	36	36
2C	38	38	38	38
2D	33	33	33	33
2E	39	39	39	39
2F	44	44	44	44
30	31	31	31	31
31	31	32	33	34
32	XX	XX	XX	XX
33	00	00	00	00
34	00	00	00	00
	Processor Type			
6B	38	38	38	38
6C	36	36	36	36
6D	34	34	34	34
6E	30	30	31	31
6F	44	44	44	44
	NAND Flash Size			
91	0E	0E	0F	0F

A.11 SPD Contents for MVME7100ET Boards

The following table describes the SPD data to be programmed into U50 and U51.

Table A-6 SPD Contents

Value	Offset	Description
00 (0x00)	80	Number of Serial PD Bytes written during module production: 0x80 = 128 bytes. Refer to Note 1.
01 (0x01)	08	Total Number of Bytes in Serial PD Device: 0x08 = 256 bytes. Refer to Note 2.
02 (0x02)	08	Fundamental Memory Type (FPM, EDO, SDRAM): 0x08 = DDR2 SDRAM
03 (0x03)	0E	Number of Row Addresses on this assembly: 0x0E = A0-A13
04 (0x04)	0A	Number of Column Addresses on this assembly: 0x0A = A0-A9
05 (0x05)	00	Number of DIMM Banks: 0x00 = one bank
06 (0x06)	48	Data Width of this assembly: 0x48 = 72 bits
07 (0x07)	00	Reserved
08 (0x08)	05	Voltage Interface Level of this assembly: 0x05 = SSTL 1.8 V
09 (0x09)	30	SDRAM Cycle time at Maximum Supported CAS Latency (CL), CL=X: 0x30 = 3.0ns. Refer to Note 3.
10 (0x0A)	45	SDRAM Access time from Clock at Maximum Supported CAS Latency (CL), CL=X: 0x45 = 0.45ns. Refer to Note 3.
11 (0x0B)	02	DIMM configuration type (Non-parity, Parity or ECC): 0x02 = ECC
12 (0x0C)	81	Refresh Rate/Type: 0x81= 3.9us. Refer to Notes 3 and 4.
13 (0x0D)	08	Primary SDRAM Width: 0x08 = 8 bits
14 (0x0E)	08	Error Checking SDRAM Width: 0x08 = 8 bits
15 (0x0F)	00	Reserved
16 (0x10)	0C	SDRAM Device Attributes - Burst Lengths Supported: 0x0C = 4, and 8 burst lengths

Table A-6 SPD Contents (continued)

Value	Offset	Description
17 (0x11)	08	SDRAM Device Attributes - Number of Banks on SDRAM Device: 0x08 = 8 banks. Refer to Note 3.
18 (0x12)	38	SDRAM Device Attributes - CAS Latency: 0x38 = CAS latency 3, 4, and 5. Refer to Note 3.
19 (0x13)	01	DIMM Mechanical Characteristics
20 (0x14)	02	DIMM Type Information
21 (0x15)	00	SDRAM Module Attributes
22 (0x16)	07	SDRAM Device Attributes - General: 0x00 = PASR, ODT and Weak Driver. Refer to Note 3.
23 (0x17)	3D	Minimum Clock Cycle at CLX-1: 0x3D = 3.75ns. Refer to Note 3.
24 (0x18)	50	Maximum Data Access Time (t AC) from Clock at CLX-1: 0x50 = 0.50ns. Refer to Note 3.
25 (0x19)	50	Minimum Clock Cycle at CLX-2: 0x50 = 5.0 Ns. Refer to Note 3.
26 (0x1A)	60	Maximum Data Access Time (t AC) from Clock at CLX-2: 0x60 = 0.60ns. Refer to Note 3.
27 (0x1B)	3C	Minimum Row Precharge Time (t RP): 0x3C = 15ns. Refer to Note 3.
28 (0x1C)	1E	Minimum Row Active to Row Active delay (t RRD): 0x1E = 7.5ns. Refer to Note 3.
29 (0x1D)	3C	Minimum RAS to CAS delay (t RCD): 0x3C = 15ns. Refer to Note 3.
30 (0x1E)	2D	Minimum RAS Pulse width (t RAS): 0x2D = 45ns. Refer to Note 3.
31 (0x1F)	01	Module Bank Density: 0x01= 1GB
32 (0x20)	20	Address and Command Setup Time Before Clock (t IS): 0x20 = 0.20ns. Refer to Note 3.
33 (0x21)	28	Address and Command Hold Time After Clock (t IH): 0x28 = 0.28ns. Refer to Note 3.

Table A-6 SPD Contents (continued)

Value	Offset	Description
34 (0x22)	10	Data Input Setup Time Before Clock (t DS): 0x10 = 0.1ns. Refer to Note 3.
35 (0x23)	18	Data Input Hold Time After Clock (t DH): 0x18 = 0.18ns. Refer to Note 3.
36 (0x24)	3C	Write Recovery Time (t WR): 0x3C = 15ns
37 (0x25)	1E	Internal Write to Read Command Delay (t WTR): 0x1E = 7.5ns
38 (0x26)	1E	Internal Read to Precharge Command Delay (t RTP): 0x1E = 7.5ns
39 (0x27)	00	Reserved
40 (0x28)	06	Extension of Byte 41 and 42
41 (0x29)	3C	Minimum Active to Active/Auto Refresh Time (t RC) 0x3C = 60ns
42 (0x2A)	7F	Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC) 0x7F = 127.5ns
43 (0x2B)	80	Maximum Cycle Time (t CK max) 0x80 = 8ns
44 (0x2C)	18	DQS-DQ Skew for DQS and associated DQ signals (t DQSQ max) 0x18 = 0.240ns
45 (0x2D)	22	Read Data Hold Skew Factor (t QHS) 0x22 = 0.340ns
46 (0x2E)	00	PLL Relock Time
47 (0x2F)	50	Tcasemax: 0x50 = 95 degree max case temperature
48 (0x30)	00	Not Used
49 (0x31)	03	0x03 = Double refresh mode bit and High temperature self-refresh
50 (0x32)	00	Not Used
51 (0x33)	00	Not Used
52 (0x34)	00	Not Used
53 (0x35)	00	Not Used
54 (0x36)	00	Not Used
55 (0x37)	00	Not Used
56 (0x38)	00	Not Used
57 (0x39)	00	Not Used

Table A-6 SPD Contents (continued)

Value	Offset	Description
58 (0x3A)	00	Not Used
59 (0x3F)	00	Not Used
60 (0x3C)	00	Not Used
61 (0x3D)	00	Not Used
62 (0x3E)	12	SPD Revision 0x12 = revision level 1.2
63 (0x3F)	xx	Checksum for bytes 0 - 62. Refer to Section 0
64 (0x40)	00	Manufactures JEDEC ID Code. Refer to Note 5.
65 (0x41)	00	
66 (0x42)	00	
67 (0x43)	00	
68 (0x44)	00	
69 (0x45)	00	
70 (0x46)	00	
71 (0x47)	00	
72 (0x48)	00	Module Manufacturing location. Refer to Note 5.
73 (0x49)	00	Module Part Number. Refer to Note 5.
74 (0x4A)	00	
75 (0x4B)	00	
76 (0x4C)	00	
77 (0x4D)	00	
78 (0x4E)	00	
79 (0x4F)	00	

Table A-6 SPD Contents (continued)

Value	Offset	Description
80 (0x50)	00	
81 (0x51)	00	
82 (0x52)	00	
83 (0x53)	00	
84 (0x54)	00	
85 (0x55)	00	
86 (0x56)	00	
87 (0x57)	00	
88 (0x58)	00	
89 (0x59)	00	
90 (0x5A)	00	
91 (0x5B)	00	Module Revision Code. Refer to Note 5.
92 (0x5C)	00	
93 (0x5D)	00	Module Manufacturing Date. Refer to Note 5.
94 (0x5E)	00	
95 (0x5F)	00	Module Serial Number. Refer to Note 5.
96 (0x60)	00	
97 (0x61)	00	
98 (0x62)	00	
99 (0x63)	00	Manufacturer's Specific Data. Refer to Note 5.
:	:	
127 (0x7F)	00	

NOTES: Notes

1. This will typically be programmed as 128 bytes.
2. This will typically be programmed as 256 bytes.
3. From datasheet.
4. High order bit is self refresh “flag”. If set to “1”, the assembly supports self refresh.
5. Reserved.

Related Documentation

B.1 Penguin Solutions Documentation

Technical documentation can be found by using the Documentation Search at *https://www.penguinsolutions.com/edge/support/* or you can obtain electronic copies of documentation by contacting your local sales representative.

Table B-1 Penguin Solutions Documentation

Document Title	Document Number
MVME7100 Data Sheet	MVME7100-DS
MVME7100ET Single Board Computer Installation and Use	6806800K87
MOTLoad Firmware Package User's Manual	6806800C24

B.2 Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-2 Manufacturer's Publications

Document Title and Source	Publication Number
AMD	
Data Sheet S29GLxxxN MirrorBitTM Flash Family S29GL512N, S29GL256N, S29GL128N 512 Megabit, 256 Megabit, and 128 Megabit, 3.0 Volt-only Page Mode Flash Memory featuring 110 nm MirrorBit process technology	Revision A Amendment 4 May 13, 2004
Atmel Corporation	
2-Wire Serial EEPROM 32K (4096 x 8), 64K (8192 x 8) AT24C32C, AT24C64C	5174B-SEEPR-12/06
2-Wire Serial EEPROM 512K (65,536 x 8) AT24C512	Rev. 1116K-SEEPR-1/04
NXP Corporation	

Table B-2 Manufacturer's Publications (continued)

Document Title and Source	Publication Number
MC864xD Integrated Host Processor Reference Manual	
MC864xD Errata	
MC864xD Integrated Processor Hardware Specifications	
NXP MR2A16AVYS35 512 KB MRAM	
Texas Instruments	
Data Sheet SN74VMEH22501A 8-bit Universal Bus Transceiver and Two 1-bit Bus Transceivers with Split LVTTL Port, Feedback Path, and 3-state Outputs	SCES620 Revised Dec 2004
Exar	
ST16C554DIQ64 Quad UART with 16-Byte FIFO's	Version 4.0.1 June 2006
Maxim Integrated Products	
DS1375 Serial Real-Time Clock	REV: 121203
MAX3243EEAI ±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 250kbps, RS-232 Transceivers with AutoShutdown	19-1283 Rev 6 9/05
MAX811/MAX812 4-Pin µP Voltage Monitors With Manual Reset Input	19-0411 Rev 3 3/99
On Semi device ADT7461	ADT7461/D, Rev 4, January 2009
IDT	
Tsi148-133ILY PCI/X-to-VME Bus Bridge User Manual	FN 80A3020_ MA001_13
Broadcom Corporation	

Table B-2 Manufacturer's Publications (continued)

Document Title and Source	Publication Number
BCM5482S 10/100/1000BASE-T Gigabit Ethernet Transceiver	5482S-DS09-R 2/13/09
PLX Technology	
PEX 8112AA ExpressLane PCI Express-to-PCI Bridge Data Book	Version 1.2
ExpressLane PEX 8114BC PCI Express-to-PCI/PCI-X Bridge Data Book	Version 3.0
ExpressLane PEX 8525AA 5-Port/24-Lane Versatile PCI Express Switch Data Book	Version 0.95

B.3 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-3 Related Specifications

Organization and Document	Document Number
VITA Standards Organization	
VME64	ANSI/VITA 1-1994
VME64 Extensions	ANSI/VITA 1.1-1997
2eSST Source Synchronous Transfer	ANSI/VITA 1.5-2003
Processor PMC	ANSI/VITA32-2003
PCI-X for PMC and Processor PMC	ANSI/VITA39-2003
PMC I/O Module (PIM) Draft Standard	VITA 36 Draft Rev 0.1 July 19, 1999
Connector Current Capacity	ANSI/VITA 1.7-2003

Table B-3 Related Specifications (continued)

Organization and Document	Document Number
Universal Serial Bus	
Universal Serial Bus Specification	Revision 2.0 April 27, 2000
PCI Special Interest Group	
PCI Local Bus Specification, Revision 2.2	PCI Rev 2.2 December 18, 1998
PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specification, Revision 2.0a	PCI-X EM 2.0a August 22, 2003
PCI-X Protocol Addendum to the PCI Local Bus Specification, Revision 2.0a	PCI-X PT 2.0a July 22, 2003
Institute for Electrical and Electronics Engineers, Inc.	
Draft Standard for a Common Mezzanine Card Family: CMC	P1386 - 2001
Draft Standard Physical and Environmental Layer for PCI Mezzanine Cards: PMC	P1386 - 2001

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